

**REMARKS**

In the present Amendment, Claims 8 and 11-14 have been amended to recite that the Si-layer is a doped Si-layer. Support for the amendment is found, for example, in the paragraph bridging pages 10 and 11 of the specification. No new matter has been added, and entry of the Amendment is respectfully requested.

Claims 8-14 are pending.

At page 2 of the Action, Claims 8-13 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Fitzgerald (US 2002/0052061) in view of JP 52-106380 (Abstract, “JP ‘380”).

At page 3 of the Action, Claim 14 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Fitzgerald in view of JP ‘380, and further in view of Waldrop et al. (US 4,999,685).

Applicant submits that the above two rejections should be withdrawn because Fitzgerald, JP ‘380 and Waldrop et al. do not disclose or render obvious the present claimed invention, either alone or in combination.

Independent Claims 8 and 14 as amended recite “laminating required compound semiconductor thin film crystal layers on a semiconductor substrate by epitaxial growth to obtain a III-V group compound semiconductor single crystal; forming a doped Si-layer on said III-V group compound semiconductor single crystal by epitaxial growth, wherein said steps are performed in a same epitaxial growth furnace.”

Fitzgerald teaches a silicon wafer with embedded optoelectronic material for monolithic OEIC. One example of the production method is in Fig. 3 (shown below) ([0026]). In the Figure, layer **302** is a Ge layer, layer **306** is a Si cap layer, layer **310** is an insulating layer, layers **304** and **308** are Si substrates.

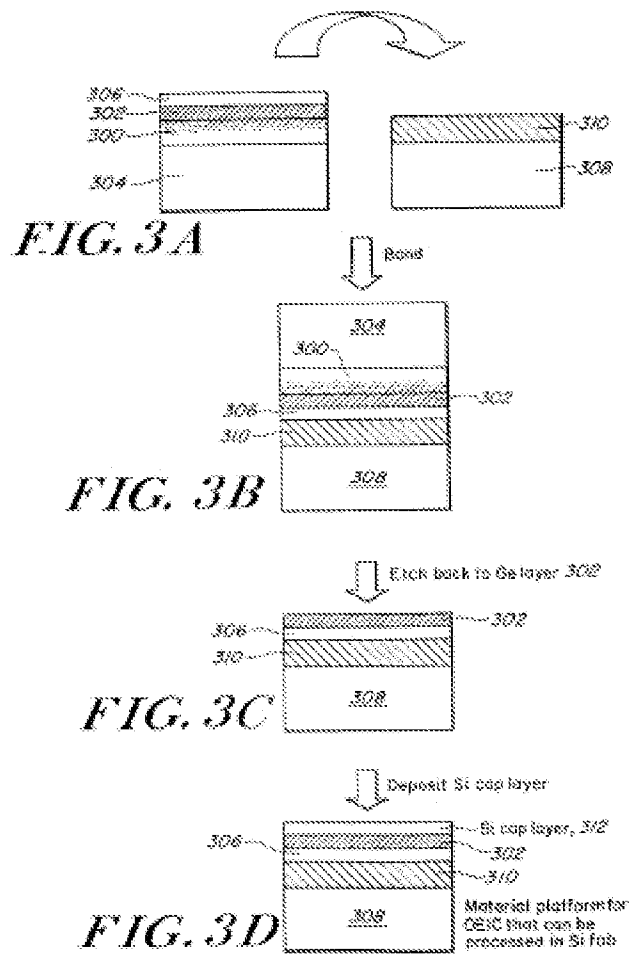


Fig. 3 of Fitzgerald

However, the Si layers in Fitzgerald are not doped. That is, Fitzgerald does not teach or suggest forming a doped Si-layer on the III-V group compound semiconductor single crystal by epitaxial growth, as required by the present claims.

JP '380 is cited to show that it is known in the art to sequential grow a plurality of III-V group compound semiconductor layers in the same epitaxial growth furnace. Waldrop et al. is relied upon as teaching depositing a metal-to-semiconductor contact, such as Au, Cr or Ti, on a heavily doped p-type layer of silicon and that the interface layer is deposited on gallium arsenide (abstract). JP '380 and Waldrop et al. do not make up for the deficiencies of Fitzgerald.

Further, as explained in the Response filed October 21, 2009, when a semiconductor is formed, a very small amount of impurities often causes significant problems. In the technical field relating to the present invention, the III-V group compound can become an impurity for Si. Based on this common knowledge, a person skilled in the art would have been concerned that the presence of the III-V group compound would adversely affect the products as an impurity. Accordingly, a person skilled in the art would not have conceived of sequentially conducting the growth of the III-V group compound semiconductor layer and the IV group semiconductor layer in the same growth furnace.

However, the present inventor has accomplished the present invention by sequentially conducting the growth of the III-V group compound semiconductor layer and the IV group semiconductor layer in the same furnace, and the present claimed invention provides excellent ohmic electrodes.

Fitzgerald, JP '380 and Waldrop et al., either alone or in combination, do not teach or suggest the superior results provided by the present claimed invention.

Accordingly, the present claims are not obvious and are patentable over Fitzgerald, JP '380 and Waldrop et al., either alone or in combination.

In view of the above, reconsideration and withdrawal of the §103(a) rejections based on Fitzgerald, JP '380 and Waldrop et al. are respectfully requested.

Allowance is respectfully requested. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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**23373**

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